Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **CT**
2. **EXT CLOCK**
3. **N/C**
4. **DRIVER B**
5. **DRIVER A**
6. **N/C**
7. **GND**
8. **RT**
9. **VREF**
10. **INPUT +**
11. **INPUT –**
12. **COMP**
13. **STATUS OUTPUT**
14. **+ VIN**

**.072”**

**.103”**

**2 1 14 13**

**4**

**5**

**12**

**11**

**10**

**7 8 9**

**U**

**I**

**C**

**C**

**9**

**3**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: UICC93**

**APPROVED BY: DK DIE SIZE .072” X .103” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: UC2901**

**DG 10.1.2**

#### Rev B, 7/1